REMARKS

The claim objections set forth in paragraphs 4-7 of the office action have been cured by appropriate amendments.

The objection to the drawing is not understood. Referring to claim 1, the multiplexer to multiplex said lower data rate and control information and transmit said data and control information externally of said integrated circuit is implemented by the serializer 24 in Figure 1. Therefore it is not believed that there is any deficiency in the drawing. It is believed that the same analysis applies to claims 14 and 23.

Therefore reconsideration is respectfully requested.

The office action suggests that Kanekawa utilizes a highly dielectric capacitor. The Examiner suggests that Figure 6 indicates that the capacitor is a separate integrated circuit. But this does not seem to be the case. In other words, there is nothing to indicate that what is shown in Figure 6 is its own separate integrated circuit. It is equally possible that what is shown in Figure 6 is simply a portion of a circuit, such as an integrated circuit. This is borne out by Figure 6B. Moreover, it does not appear that the capacitor could constitute the claim's second integrated circuit, which must include a demultiplexer to demultiplex said lower data rate data and said control information. Most certainly, there is no indication anywhere in Kanekawa that the items 50-2, 50-1, and 50-2 are on monolithic integrated circuits.

While it is possible to make the demultiplexer a separate integrated circuit, one skilled in the art must learn from the prior art some reason to do so. Normally, as technology progresses, items are not de-integrated, they are integrated on fewer and fewer chips.

The Examiner suggests that the 50-1, and 50-2 "could be" formed for a separate integrated circuit. Of course, anything is possible. The only relevant issue though is what is actually taught. Since doing this is only devined from Kanekawa with the benefit of hindsight reasoning, a *prima facie* rejection is not made out.

Likewise, concerning the argument that "with the advance of IC technology, one of ordinary skill in the art will appreciate that the cited regions can be formed on an integrated circuit," it is not known what advance in IC technology that the Examiner could be referring to. As integrated circuits advances fewer, not more, separate integrated circuits are used.

What is missing from the prior art is the rationale to do so in the specific application set forth herein. Nothing in the art in any way suggests the claimed solution.

Both Yukutake and Kanekawa teach away from the claimed invention because they effectively suggest putting everything on one integrated circuit.

Therefore, reconsideration of the rejection is respectfully requested.

Respectfully submitted,

Date: October 18, 2004

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